In the Specification:

Please amend the paragraph beginning at page 40, line 8 to read as follows:

The NOR gate **56** includes PMOS pull-up transistors P27 and P28 **[[**P25 and P26**]]** and NMOS pull-down transistors N28 and N29 that receive a pair of input signals. The NOR gate **56** also includes a PMOS pull-up transistor P29 that operates to pull-up an output of the NOR gate **56** in-sync with a leading high-to-low edge of the look-up enable signal LUENB_c. An NMOS transistor N30 is also provided for enabling the NOR gate **56** in-sync with a trailing low-to-high edge of the look-up enable signal LUENB_c. The output of the NOR gate **56** is provided to an input of an inverter I7 and to a pair of PMOS precharge transistors. One of these PMOS precharge transistors (shown as P30) has a drain terminal that is electrically connected to the upper match line segment ML0_c. The NOR gate **56** operates to drive the input of inverter I7 low whenever one (or both) of the lower match line signals ML0_b or ML1_b is high at the end of the preceding stage of the pipelined search operation. This driving operation, which results in a precharge of both of the upper match line segments ML0_c and ML1_c and the upper pseudo-ground line segment PGND_c, is performed in-sync with the rising edge of the look-up enable signal LUENB_c. After precharge, the upper pseudo-ground line segment PGND_c will be pulled low to commence the next stage of the pipelined search operation in-sync with a leading high-to-low edge of the active low look-up enable signal LUENB_c. When this occurs, the precharged upper match line segment ML0_c will be pulled low by NMOS pull-down transistors N31 and N32 if the lower match line segment ML0_b was inactive at a logic 0 level (to thereby indicate a miss condition in the preceding segment(s) of CAM cells) when the leading low-to-high edge of the look-up strobe signal LUSTB_b was received by the 4T inverter.